

Description

[STRUCTURE APPLIED TO A PHOTOLITHOGRAPHIC PROCESS AND METHOD FOR FABRICATING A SEMICONDUCTOR DEVICE]

BACKGROUND OF INVENTION

[0001] Field of the Invention

[0002] The present invention relates to a structure applied to a photolithographic process and a method for fabricating a semiconductor device. More particularly, the present invention relates to a structure applied to a photolithographic process for improving critical dimensions uniformity and a method that utilizes the structure to fabricate a semiconductor device.

[0003] Description of the Related Art

[0004] In the fabrication of a semiconductor device, a number of photolithographic processes needs to be carried out. Since each photolithographic process is going to affect

the final quality of the semiconductor device, photolithography is a very important process. For example, accuracy of the photolithographic process is a major factor that determines the highest possible circuit density and the ultimate reliability of an integrated circuit. Furthermore, the photolithographic process affects the positioning and uniformity of metallic interconnects and via plugs connection with transistor significantly.

[0005] However, in a conventional photolithographic process, the photoresist layer can hardly absorb all light emitted from the photo-exposure light source. Consequently, a portion of the incoming light will penetrate through the photoresist layer and reflect from the substrate. The incoming light may interfere constructive or destructively with the reflected light to produce standing waves. Under such circumstances, the profile of the photoresist layer after photoresist patterning will be fuzzy.

[0006] To resolve the back reflection problem, an anti-reflection coating is formed underneath the photoresist layer (that is, form an anti-reflection layer between the photoresist layer and an underlying film layer) to absorb the light that penetrates through the photoresist layer during a photo-exposure. In the presence of the anti-reflection coating,

interference between incoming and reflected light is minimized. In general, the anti-reflection coating is fabricated using a dielectric material such as silicon nitride, silicon oxynitride or an organic material with high light absorption properties.

[0007] However, the light absorption coefficients of all these materials are often insufficiently high to absorb most of the incoming light. In other words, a portion of the incoming light still penetrates through the anti-reflection coating and underlying film layers and gets reflected by the substrate surface to interfere with the incoming light. Moreover, the critical dimensions of a photoresist pattern are often affected by any varying of thickness in the film layer underneath the anti-reflection coating. Ultimately, critical dimensions of the photoresist pattern will not be uniform.

SUMMARY OF INVENTION

[0008] Accordingly, at least one objective of the present invention is to provide structure applied to a photolithographic process for stopping light emitted from a light source during a photo-exposure from penetrating through a film layer to reach a substrate surface. Hence, variation in the thickness of the film layer has very little effect on the critical dimensions of the photolithographic process.

[0009] At least a second objective of this invention is to provide a method of fabricating a semiconductor device that deploys the aforementioned photolithographic processing structure so that the device can have highly uniform critical dimensions.

[0010] To achieve these and other advantages and in accordance with the purpose of the invention, as embodied and broadly described herein, the invention provides a structure applied to a photolithographic process. The structure comprises a substrate having at least a film layer thereon. Furthermore, an optical isolation layer, an anti-reflection coating and a photoresist layer are set up over the substrate sequentially. The optical isolation layer stops incoming light from penetrating through the layer. In one embodiment, the optical isolation layer has a light absorbing coefficient larger than 1.8. Hence, the amount of light that can reach the surface of the substrate during a photo-exposure process is greatly reduced.

[0011] This invention also provides a method of fabricating a semiconductor device. First, a substrate is provided. Thereafter, at least a film layer, an optical isolation layer, an anti-reflection coating and a photoresist layer are sequentially formed over the substrate. A photolithographic

process is carried out to pattern the photoresist layer so that a portion of the anti-reflecting coating is exposed. Using the patterned photoresist layer as a mask, the anti-reflection coating and the optical isolation layer are patterned and openings are formed in the film layer above the substrate.

[0012] This invention also provides an alternative method of fabricating a semiconductor device. First, a substrate having at least a film layer, an optical isolation layer, an anti-reflection coating and a photoresist layer already sequentially formed thereon is provided. Thereafter, a photolithographic process is carried out to pattern the photoresist layer so that a portion of the anti-reflecting coating is exposed. Using the patterned photoresist layer as a mask, the anti-reflection coating and the optical isolation layer are patterned. The patterned photoresist layer and the patterned anti-reflection coating are removed. Finally, using the optical isolation layer as a mask, an etching operation is carried out to form openings in the film layer.

[0013] In the aforementioned photolithographic processing structure, an optical isolation layer is set up underneath the photoresist layer. Hence, during photo-exposure, light from a light source can hardly penetrate through the

film layer to get a back reflection from the substrate surface. In other words, thickness of the film layer underneath the photoresist layer has very little effect on the critical dimensions of the photolithographic process.

[0014] In addition, critical dimensions of the semiconductor device in subsequent fabrication process will improve due to a better control of the critical dimensions during the photolithographic process. Furthermore, the optical isolation layer in the aforementioned structure may serve as an etching stop layer or a polishing stop layer as well.

[0015] It is to be understood that both the foregoing general description and the following detailed description are exemplary, and are intended to provide further explanation of the invention as claimed.

BRIEF DESCRIPTION OF DRAWINGS

[0016] The accompanying drawings are included to provide a further understanding of the invention, and are incorporated in and constitute a part of this specification. The drawings illustrate embodiments of the invention and, together with the description, serve to explain the principles of the invention.

[0017] Figs. 1A through 1E are schematic cross-sectional views showing the progression of steps for forming the contacts

of metallic interconnects according to a first preferred embodiment of this invention.

[0018] Figs. 2A and 2B are schematic cross-sectional views showing a portion of the steps for producing the contacts of metallic interconnects according to another preferred embodiment of this invention.

DETAILED DESCRIPTION

[0019] Reference will now be made in detail to the present preferred embodiments of the invention, examples of which are illustrated in the accompanying drawings. Wherever possible, the same reference numbers are used in the drawings and the description to refer to the same or like parts.

[0020] In the following description, the process of fabricating the contacts of metallic interconnects is used as an example to show how the structure of this invention can be applied to a photolithographic process.

[0021] Figs. 1A through 1E are schematic cross-sectional views showing the progression of steps for forming the contacts of metallic interconnects according to a first preferred embodiment of this invention. As shown in Fig. 1A, a dielectric layer 102, an optical isolation layer 104, an anti-reflection coating 106 and a photoresist layer 108 are se-

quentially formed over a substrate 100. The dielectric layer 102 serves as an inter-layer dielectric layer for the metallic interconnects and covers a plurality of semiconductor devices (not shown) and other film layers (not shown) already formed on the substrate 100.

[0022] The optical isolation layer 104 preferably has a light absorbing coefficient greater than 1.8. Furthermore, the optical isolation layer 104 is fabricated using a metallic material or a conductive material including polysilicon, tungsten or aluminum, for example. The anti-reflection coating 106 is fabricated using an inorganic material such as silicon nitride or silicon oxynitride or an organic material suitable for anti-reflection.

[0023] As shown in Fig. 1B, a photolithographic process is carried out to pattern the photoresist layer 108 into a patterned photoresist layer 108a so that a portion of the anti-reflection coating 106 is exposed.

[0024] Note that the anti-reflecting coating 106 is able to absorb some of the light passing through the photoresist layer 108 during the photo-exposure in the photolithographic process. Any residual light not absorbed by the anti-reflection coating 106 is completely blocked by the optical isolation layer 104. The optical isolation layer 104 has a

high light absorption coefficient so that most of the light passing through the anti-reflection coating 106 is absorbed. Furthermore, the optical isolation layer 104 reflects a portion of the light back onto the anti-reflection coating 106 so that the anti-reflection coating 106 can reabsorb the light. As a result, the optical isolation layer 104 is able to block any light heading towards the underlying dielectric layer 102. Consequently, any variation in thickness of the dielectric layer 102 underneath the photoresist layer 108 has little effect on the critical dimensions of the photolithographic process. That means, the critical dimensions produced after the photolithographic process is highly uniform.

[0025] Aside from blocking the passage of light, the optical isolation layer 104 may serve as an etching stop layer or a polishing stop layer in a subsequent process. Details of its application are explained below.

[0026] As shown in Fig. 1C, an etching process is carried out using the patterned photoresist layer 108a as a mask to form a patterned anti-reflection coating 106a, an optical isolation layer 104a and a plurality of contact openings 110 in the dielectric layer 102.

[0027] Note that a definite thickness of the patterned photoresist

layer 108a, the anti-reflection coating 106a or the entire patterned photoresist layer 108a and the anti-reflection coating 106a may be etched away after the etching operation. However, because the optical isolation layer 104 is fabricated using a metallic or polysilicon material in this invention, the dielectric layer has an etching rate much higher than the optical isolation layer 104. Even though the patterned photoresist layer 108a and the patterned anti-reflection coating 106a are completely etched away, the optical isolation layer 104a can still serve as an etching mask to complete the patterning process and form the contact openings 110 in the dielectric layer 102.

[0028] As shown in Fig. 1D, the patterned photoresist layer 108a and the patterned anti-reflection coating 106a are removed. If the patterned anti-reflection coating 106a is fabricated using organic material, the patterned anti-reflection coating 106a and the photoresist layer 108a can be removed together in the same process. However, if the patterned anti-reflection coating 106a is fabricated using inorganic material such as silicon nitride or silicon oxynitride, a separate etching process must be carried out after removing the photoresist. Thereafter, a material layer 112 is formed over the patterned optical isolation layer

104a so that the contact openings 110 are completely filled. The material layer 112 is fabricated using a metallic material such as tungsten, copper or a conductive material.

[0029] As shown in Fig. 1E, a chemical-mechanical polishing process is carried out to remove the material layer 112 above the patterned optical isolation layer 104a and expose the optical isolation layer 104a. Hence, contacts 114 are formed in the dielectric layer 102. Note that the patterned optical isolation layer 104a can serve as a polishing stop layer in the chemical-mechanical polishing process.

[0030] If the contact openings 110 have a high aspect ratio, another series of step may be performed to form the contact openings 110 after patterning the photoresist layer 108a (as shown in Fig. 1B). The method is explained as another embodiment of this invention below.

[0031] Figs. 2A and 2B are schematic cross-sectional views showing a portion of the steps for producing the contacts of metallic interconnects according to another preferred embodiment of this invention. As shown in Fig. 2A, after forming the patterned photoresist layer 108a as shown in Fig. 1B, an etching operation is carried out using the patterned photoresist layer 108a as a mask to form a pat-

terned anti-reflection coating 106a and a patterned optical isolation layer 104a.

[0032] As shown in Fig. 2B, the patterned photoresist layer 108a and the patterned anti-reflection coating 106a are removed. Thereafter, using the patterned optical isolation layer 104a as a mask, an etching operation is carried out to form contact openings 110 in the dielectric layer 102. Since the patterned photoresist layer 108a and the patterned anti-reflection coating 106a are removed before etching the dielectric layer 102, the aspect ratio of the contact openings 110 is greatly reduced. Hence, the contact openings 110 are easier to form.

[0033] After forming the contact openings 110, conductive material is deposited into the contact openings 110 to form the contact as in the first embodiment (refer to Figs. 1D and 1E).

[0034] Since the optical isolation layer effectively stops any light from going to the film layer underneath, any variation of thickness of the film layer underneath the photoresist layer will not affect the critical dimensions of the photolithographic process. Furthermore, the optical isolation layer may serve as a stopping layer in a subsequent chemical-mechanical polishing process or an etching pro-

cess.

[0035] Although the process of fabricating the contacts of metallic interconnects is used in the two aforementioned embodiments, the applications of the photolithographic processing structure according to this invention are not limited as such. In fact, any photolithographic process for fabricating a semiconductor device may utilize the structure to improve the uniformity of critical dimensions.

[0036] It will be apparent to those skilled in the art that various modifications and variations can be made to the structure of the present invention without departing from the scope or spirit of the invention. In view of the foregoing, it is intended that the present invention cover modifications and variations of this invention provided they fall within the scope of the following claims and their equivalents.